

Amendment dated August 25, 2004
Appl. No. 10/064,856
Atty. Docket No. 00100.02.0038

REMARKS

Applicant respectfully traverses and requests reconsideration.

According to the Advisory Action, the response and proposed amendments to the final Office Action were entered. However, the Advisory Action did not respond to the Applicant's arguments in the response to final Office Action.

Rejection of claims under 35 U.S.C. § 102

Claims 1, 3 through 4, 9 through 12 and 16 currently stand rejected under 35 U.S.C. § 102(b) based on U.S. Patent No. 6,243,817 (Melo).

Applicants repeat the remarks made in response to the previous Office Actions. In addition, the claims have been amended to include limitations shown in Figs. 2 through 9 indicating that the information router and the system memory are directly connected to the carrier substrate via at least one of a plurality of electrical leads. For example, Fig. 6 shows the electrical leads directly connect the plurality of system memories 262 and the ASIC 254. The electrical leads may travel through a plurality of layers 244 as described in Fig. 3 and in the Specification on page 9 lines 4 through 9. Among other advantages, directly connecting the plurality of system memories 262 and the ASIC 254 or any suitable die on the same integrated circuit 204 improves the speed of the integrated circuit 204. (Specification, page 8 lines 5 – 8, page 6 lines 1-3.)

However, as noted in the previous responses hereby incorporated by reference, Melo is directed to a computer using conventional CPU buses and PCI buses. (Melo, col. 4, lines 41–68.) Such a conventional computer architecture couples the system memory and the information router via long buses as is described in Applicant's background of the invention on pages 4 and 5 of the specification rather than via electrical leads directly connected to the carrier substrate. The claimed invention seeks to avoid the problems associated with relatively long conventional computer system buses on a printed circuit board. (Specification page 4.) These problems include inductive and capacitive effects negatively affect bus bandwidth. *Id.* Melo is silent with regards to the information router and the system memory directly connected to the carrier

CHICAGO/1307542.2 11/24/04
00100.02.0038
DRAFT

Amendment dated August 25, 2004
Appl. No. 10/064,856
Atty. Docket No. 00100.02.0038

substrate via at least one of a plurality of electrical leads. For at least the reasons above, Melo as cited fails to teach each and every element of the amended claims. Therefore, Applicants submit that the amendment to claim 1 overcomes the current rejection. Accordingly, reconsideration of amended claim 1 is respectfully requested.

Rejection of claims under 35 U.S.C. § 103(a)

Claims 5 through 8 and 13 through 15 are rejected under 35 U.S.C. § 103(a) based on Jeddeloh (United States Patent No. 6,346,446) and further in view of U.S. Patent Application No. 2003/0183934 ("Barrett").

The final Office Action on page 3 acknowledges that Jeddeloh does not disclose the die coupled to the bottom using wire bonds and flip chip technology. However, the final office action does not cite to any portion of Jeddeloh for showing where any of the remaining elements of the claims are recited. A showing of each and every element as arranged in the claims is respectfully requested. (C.F.R. § 1.104 (c) (2)). The system of Jeddeloh teaches a specific interface between the north bridge 102 and processor 112-116 across the processor bus 108 where the system memory located outside of the north bridge. As noted in the previous responses, Jeddeloh describes a prior art approach that the present invention overcomes because, among other things, the processor interface in Jeddeloh does not contain the claimed system memory, but only provides for interfacing with processors 112 through 116, across the processor bus 108 for access through the switch 124. Such a structure different results in further processing delays for transferring information across the processor bus.

Barrett is directed to multiple die in a flip chip semiconductor package (Barrett, para. 10.) Barrett describes the semiconductor package including a cache memory and a graphics controller. (Barrett, para. 12.) The combination of Jeddeloh and Barrett fails to describe an information router integrated on the standard dimension carrier substrate via at least one of the plurality of electrical leads in electrical communication with the system memory via at least one of the plurality of electrical leads directly connected to the standard dimension carrier substrate. A showing is respectfully requested. As a result, the claims are believed to be allowable for at

Amendment dated August 25, 2004
Appl. No. 10/064,856
Atty. Docket No. 00100.02.0038

least the above reasons. It is further submitted these claims contain patentable subject matter and are allowable not merely as being dependent upon an allowable base claim.

In addition, Applicants have added new claims 21, 22 and 23. New claim 21 recites, among other things, system memory integrated on the standard dimension carrier substrate via at least one of the plurality of electrical leads directly connected to the standard dimension carrier substrate, an information router integrated on the standard dimension carrier substrate in electrical communication with the system memory via at least one of the plurality of electrical leads directly connected to the standard dimension carrier substrate. Support for new claim 21 may be found in original claim 1 and, pages 7, 8 and 9 of the Specification, and Figs. 2-9. As stated above, Melo, nor the combination of Jeddelloh and Barrett contemplates, teaches or suggests a standard dimension carrier substrate for integrating system memory and an information router via a plurality of electrical leads directly connected to the standard dimension carrier substrate. As a result, claim 21 is believed to be allowable for at least the above reasons

New claim 22 further recites, wherein the information router is operative to route processing instructions between a host processor external to the standard dimension carrier substrate via a host processor bus, a co-processor external to the standard dimension carrier substrate via an external co-processor bus and system memory. Support for amended Claim 22 may be found at least on pages 2 and 3 of the specification. It is further submitted that claim 22 contains patentable subject matter and is allowable not merely as being dependent upon an allowable base claim.

Claim 23 further recites a standard dimension carrier substrate having dimensions of a width between 31mm and 41 mm inclusively and a length between 31mm and 41 mm inclusively. Support for amended claim 23 may be found on page 8 lines 19 through page 9 line 1. It is further submitted that claim 23 contains patentable subject matter and is allowable not merely as being dependent upon an allowable base claim.

Amendment dated August 25, 2004
Appl. No. 10/064,856
Atty. Docket No. 00100.02.0038

Accordingly, Applicant respectfully submits that the claims are in condition for allowance and request that a timely Notice of Allowance be issued in this case. The Examiner is invited to contact the below-listed attorney if the Examiner believes that a telephone conference will advance the prosecution of this application.

Respectfully submitted,

Date: November 26, 2004

By: Themi Anagnos / pb
Themi Anagnos
Registration No. 47,388

VEDDER, PRICE, KAUFMAN &
KAMMHOLZ, P.C.
222 North LaSalle Street
Chicago, IL 60601
Telephone: (312) 609-7870
Facsimile: (312) 609-5005
Email: tanagnos@vedderprice.com